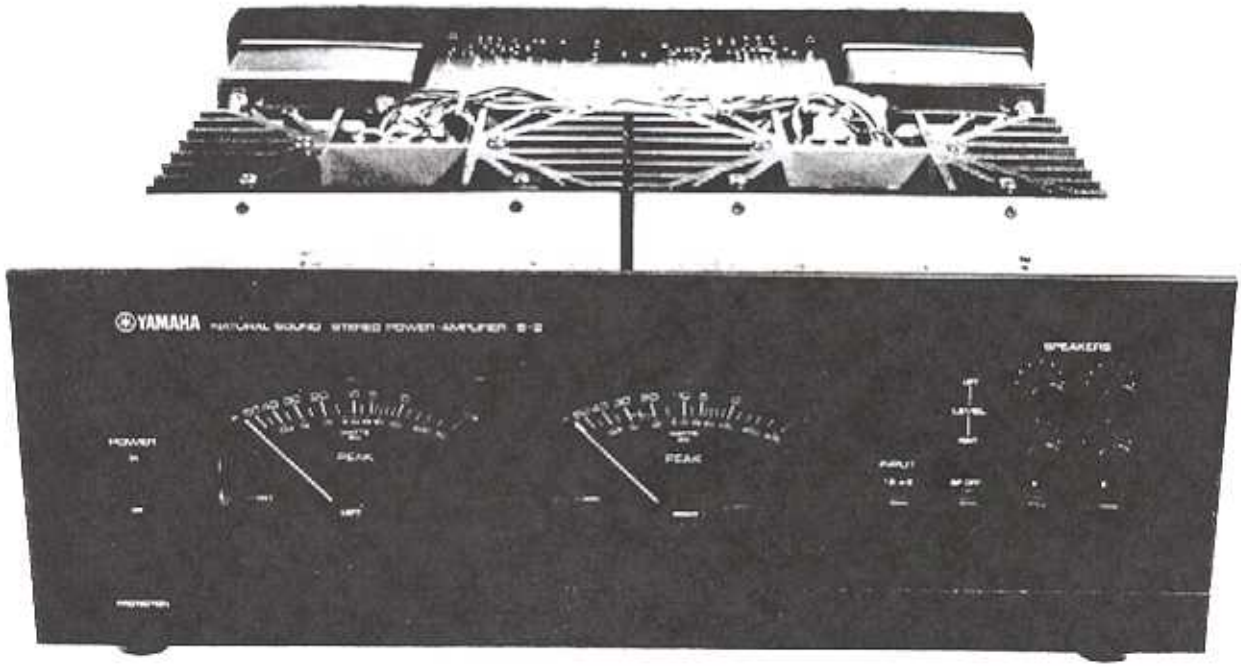


YAMAHA FET POWER AMPLIFIER

B-2

Technical Report

The New Power FETs Developed for the B-2

The power FETs developed for the B-2 are the 2SK-76 (N-channel) and the 2SJ-26 (P-channel). As well as being smaller than the high power 2SK-77 FETs used the B-I, their characteristics have been made complementary. In addition to the advantages of FETs generally, such as low input impedance and high switching speed, etc., the special B-2 FETs were developed from considerations of the ideal characteristics required of FETs to be used in fully complementrary configurations, and of how such semiconductor elements were to be manufactured and the pairing carried out.

It is widely recognised that the characteristics of semiconductors display considerable variation, and it is far from simple even to obtain closely matched elements with the *same* polarity. YAMAHA investigated exhaustively the chip size of P-channel and N-channel devices, the impurity levels, and gate mesh structure, etc., and established rigorous production controls, to achieve a wide operational range over which paired characteristics could be obtained. A special final stage of pair selection eventually yields the super-pair FETs used in the B-2. Photograph 4 shows the output characteristics of the 2SK-76 (N-ch) and 2SJ-26 (P-ch) FETs. It is clear that the B-2 power FETs have the following special features:

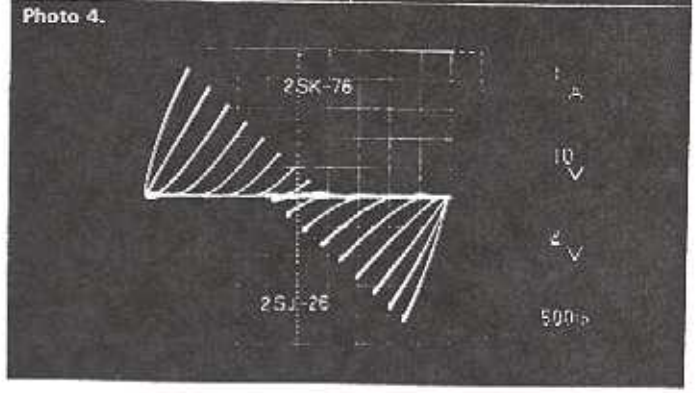
① Good complementarity,
② Good linearity is maintained over a wide operating range,
③ Voltage gain is high ($\mu \simeq 7.5$), and
④ They withstand high operating voltages, etc.

Photo 1. The 2SK-77 Power FET (B-I)

Photo 2. The 2SK-76 FET

Photo 3. The 2SJ-26 FET

Photo 4.



The technology required to develop and exploit FETs with these characteristics includes the ability to design the devices, to translate them into practical terms, to manufacture them, and particularly to grow high purity epitaxial layers of adequate depth.

The development of the B-2 commenced with the identification of the performance categories in which an audio amplifier must excel, went on to design circuits which would be capable of the required performance standards in each category, and was completed by the development of semiconductor devices (FETs) which could satisfy the severe demands of such circuits.

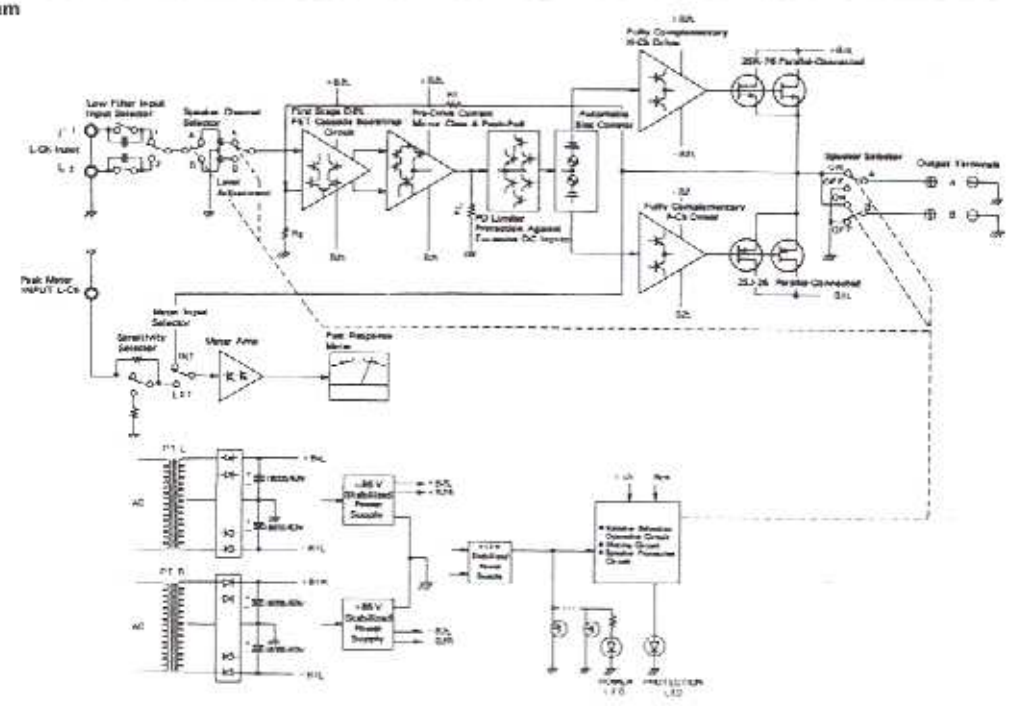
Table: Maximum Rated Performance(T_a = 25°C)

	2SK-76	2SJ-26
Drain-Gate Potential (V_{DGO})	200V	−150V
Gate-Source Potential (V_{GSO})	−40V	40V
Drain Current (I_D)	10A	−10A
Gate Current (I_G)	1A	−1A
Drain Dissipation (P_D)	100W	100W
Junction Temp. (T_j)	150°C	150°C

Variable	2SK-76		2SJ-26	
	Conditions	Value	Conditions	Value
BV_{DGO}	I_G=100μA I_S=0	200V MIN	I_G=−100μA I_S=0	−150V MIN
BV_{GSO}	I_G=−100μA I_D=0	−40V MIN	I_G=100μA I_D=0	40V MIN
I_{DGO}	V_{DG}=−100V I_S=0	10μA MAX	V_{DG}=−100V I_S=0	10μA MAX
I_{GSS}	V_{GS}=30V V_{DS}=0	−10μA MAX	V_{GS}=−30V V_{DS}=0	10μA MAX
I_{DSS}	V_{DS}=−10V V_{GS}=0	5A TYP	V_{DS}=10V V_{GS}=0	5A TYP
$V_{GS(off)}$	V_{DS}=−10V I_D=−1mA	20V MAX	V_{DS}=50V I_D=1mA	20V MAX
y_{fs}	V_{DS}=−30V I_D=−2A f=1kHz	750mσ TYP	V_{DS}=30V I_D=2A f=1MHz	750mσ TYP
μ		7.5 TYP		7.5 TYP
r_D		10Ω TYP		10Ω TYP
C_{iss}	V_{DS}=0 V_{GS}=10V f=1MHz	1000PF TYP	V_{DS}=0 V_{GS}=−10V f=1MHz	700PF TYP
C_r	V_{DG}=−50V I_S=0 f=1MHz	150PF TYP	V_{DG}=50V I_S=0 f=1MHz	100PF TYP

Circuit Structure

Fig. 1. Block Diagram



The structure consists of a first stage differential FET cascode-bootstrap circuit, a pre-drive stage with current-mirror differential push-pull amplification, a drive stage featuring fully complementary symmetrical push-pull, and an output stage using the super-pair FETs in a fully complementary configuration with parallel push-pull OCL circuitry: all stages are directly coupled.

Conventional wisdom has it that FET amplifiers suffer from low gain unless a three-stage structure is adopted, and for which distortion tends to be high. However, with the B-2, the high linearity of the output FETs, and the fact that they can be driven by very low operating power, enable a very simple circuit structure to be adopted. Combination with current-mirror circuitry and the use of all push-pull from the pre-drive through to the final output stage means that sources of distortion in both the semiconductor elements and in the circuits have been reduced until the open-loop characteristics are outstandingly good. This reduces the demand for NFB to suppress distortion. The pre-drive unit only needs to have two stages, which is in itself a factor in reducing overall distortion. This advanced circuit configuration eliminates all capacitors from the NFB loop, and, with the accompanying elimination of the input capacitor, the B-2 is DC + DC (direct coupled and operating down to direct current), with linear response to 0Hz.

1. First Stage — Pre-Drive Stage
(Voltage Amplification)

The rigorously matched super low-noise FET pair in the first stage are coupled thermally and form a differential amplifier. In direct-coupled amplifiers there is often a problem associated with temperature drift in the center or 'balance' potential which is connected to the speakers. Serious temperature drift will result in a direct current flowing through the speakers.

Fig. 3. Voltage Amplification Stage

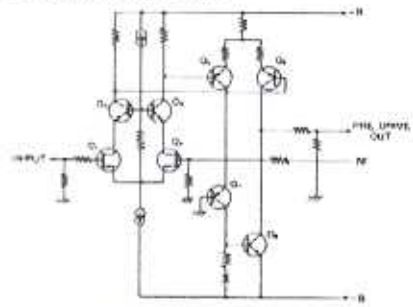


Fig. 4. Center Potential Drift

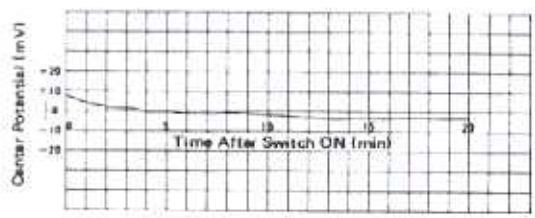
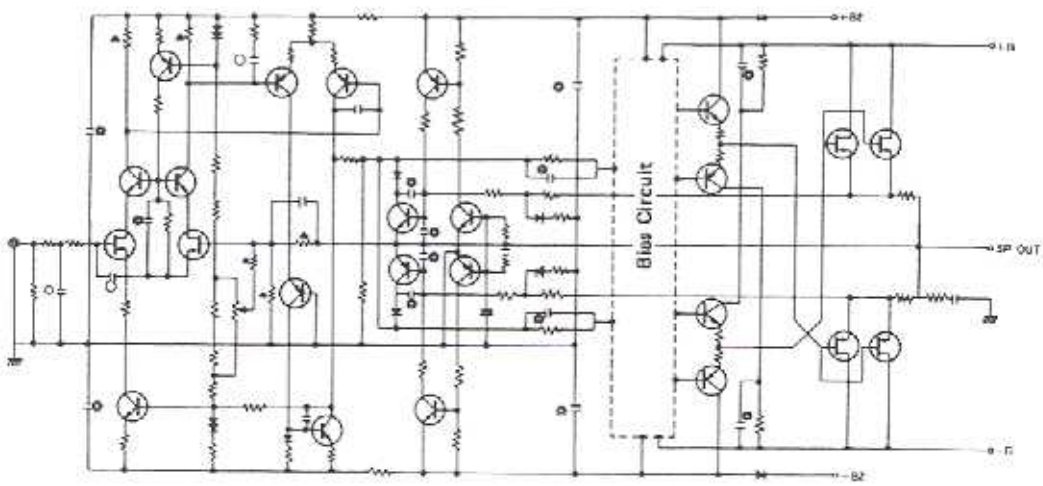


Fig. 2. Power Amplifier Circuit Diagram

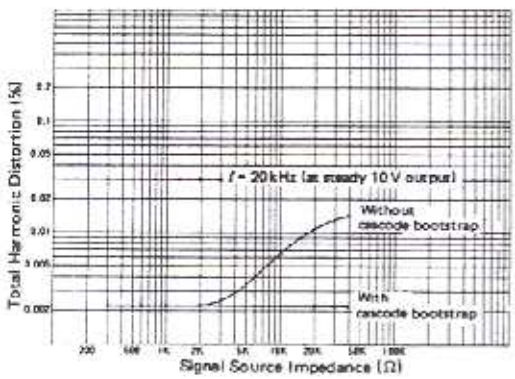


In the B-2, FETs with the high *gm* are used close to the optimum I_{DSS}, with temperature compensated constant current source bias, giving a common mode rejection ratio (CMRR) which is unusually high, and which is clear evidence of highly effective differential amplifier design. CMRR is a measure of the rejection of in-phase signal components. It is so high that the center point potential drift is exceptionally low, within 10 mV. Traces of electrical supply ripple are also cancelled, so that in combination with the super low-noise FETs, the S/N ratio is better than 115dB (IHF-A with shorted input).

Conventional amplifier design has often resulted in degraded distortion when signal source impedance rises. In particular, distortion often increases as the input volume control is reduced below maximum. This is due to the non-linear variation in spurious input signal generated by the small collector-base current which flows in transistors (drain-gate current in FETs) in the input stage. The current varies with the drain-gate potential, so that high impedance sources were subject to increased distortion.

In the B-2, this problem has been completely solved by the use of a first stage differential amplifier with cascode-bootstrap circuit assembly. This assures that the drain-gate potential does not vary, so that even if the input impedance does change, there is no increase in distortion. Adequate gain and low distortion are further secured by the following pre-drive current-mirror differential amplifier with push-pull class A operation.

Fig. 5. Reduction in Distortion Due to Cascode Bootstrap Circuit

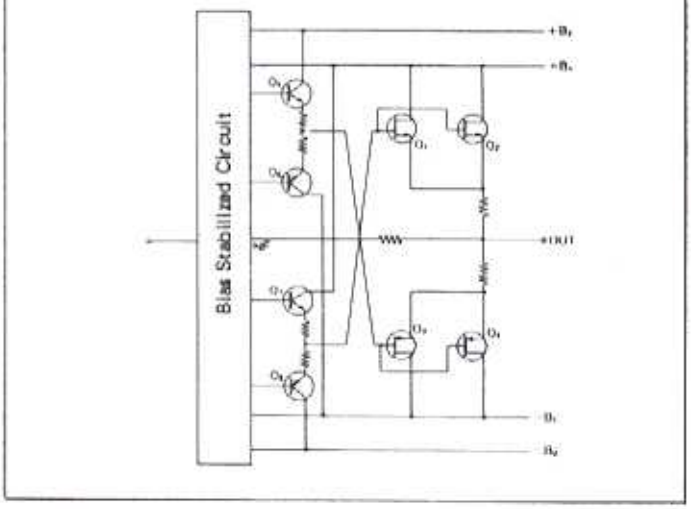


2. Drive Stage — Output Stage
(Power Amplification)

Because FETs are essentially voltage-amplifier elements, they have higher input impedances, and do not require the high power drive of bi-polar transistors. However, electrical power is required for the charge and discharge of the gate (G) to source (S) input capacity. Minimizing the time constant of the FET input capacity and the drive impedance will give the highest possible high frequency response.

In the B-2, a survey of the various drive-circuit options revealed the symmetrical push-pull circuit eventurally adopted to be the most outstandingly effective.

Fig. 6. Power Amplification Stage



- **Notes on the symmetrical push-pull drive**

'Symmetrical push-pull' involves the use of P-ch and N-ch FETs in the power stage in a fully complementary push-pull drive circuit configuration, with the following advantages:

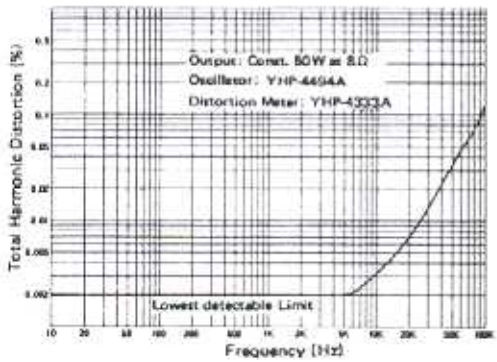
① In comparison with emitter-follower circuitry, the drive impedance is the same in both ON and OFF states, and can be considerably reduced.

② For frequencies in or near the audio band, FET input impedance is high, so that little current is required in the drive stage. At much higher frequencies, however, the input capacity requires class B operation, but the advantages of ① above are retained. (With emitter-follower circuitry, any attempt to reduce the drive impedance involves reducing the emitter resistance, so that larger currents must flow.)

③ With low requirements for drive stage current, transistors with small P_C can be used. The B-2 uses the same transistors as are used in the pre-drive stage, with a maximum P_C of approximately 1 Watt, making possible high h_{fe} and f_t. This is evidence of the extremely advantageous pre-drive design.

The output stage uses two of the YAMAHA special super-pairs of FETs in a fully complementary parallel push-pull OCL circuit. The special YAMAHA selection procedure gives FETs with extremely closely matched characteristics at low currents, so that from low power level outputs right up to very high power levels, for all frequencies, the distortion is extremely low. Large heat sinks are used, with separate units for left and right channels. No mica is used in the FETs, which are directly attached by a special process to the heat sinks, giving a thermal resistance less than half that of conventional mica construction. This assures effective heat dissipation.

Fig. 7. Frequency vs. Total Harmonic Distortion



One representative characteristic for a power amplifier is the graph of output power against total harmonic distortion. This is shown in Figure 8. A 20kHz distortion waveform is shown in Photograph 5. At 20Hz and 1kHz, from 4 Watts to 100 Watts, distortion is less than 0.005%, Even at 20kHz, distortion is still less than 0.008% from 1 Watt to 60 Watts. These are extremely good figures. Cross-over distortion has been virtually eliminated, giving smooth waveforms and superior low distortion performance. In Photograph 6, spectral analysis fails to reveal any visible harmonic distortion at all.

Fig. 8. Output Power vs. Total Harmonic Distortion

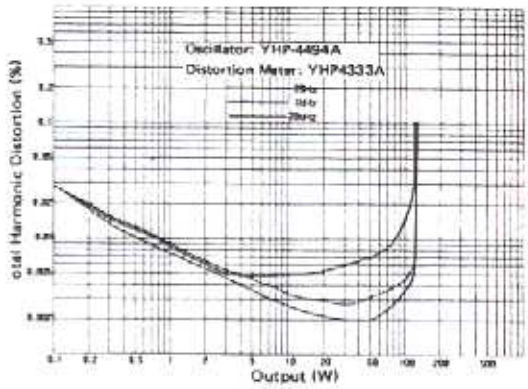


Photo 5
20kHz Sine Wave Distortion Waveform

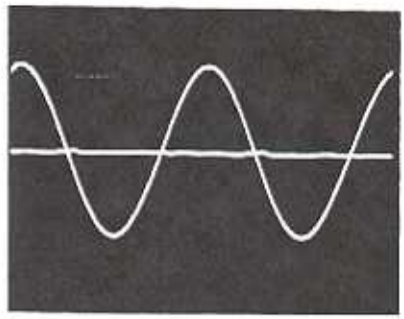


Photo 6
Noise Spectrum as Revealed by Spectral Analyzer

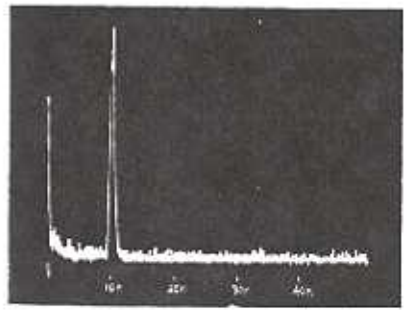
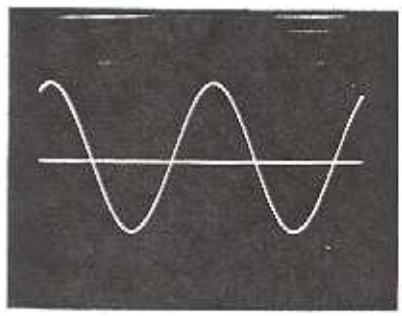


Photo 7
20Hz Sine Wave Distortion Waveform



This is clearly attributable to the use of FETs with highly linear characteristics, a sophisticated method for matching pairs, and the symmetrical push-pull drive, etc. The 20Hz waveform, in particular, reveals no ripple content, showing the inherent quality of this DC amplifier.

Figure 9 and Photograph 8 show the power bandwidth and the slew rate. The extremely high slew rate is due to the inherently high switching rate of vertical FETs and the response from DC to 100kHz (3dB below rated maximum output, with 0.1% distortion) of the symmetrical drive amplifier circuitry.

Fig. 9. Power Bandwidth

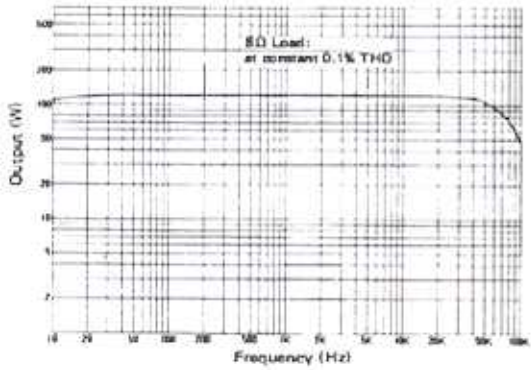


Photo 8
Slew Rate

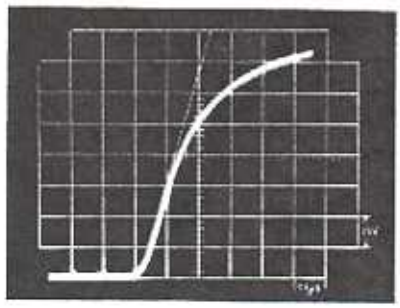
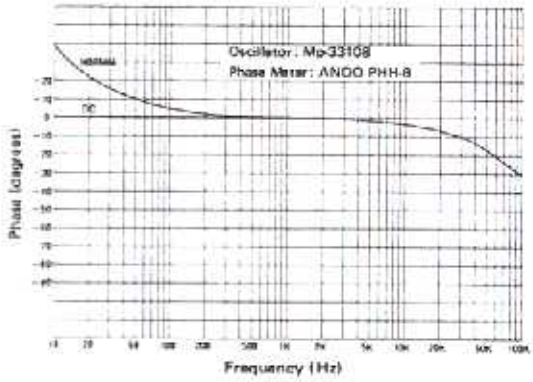


Figure 10 shows the phase deviation with frequency. The direct-coupled amplifier in the DC position gives negligable deviation down to DC. In the NORMAL position, the absence of a sub-sonic filter in this amplifier means that there is only a slight low frequency 'droop' and only +40° phase deviation at 10Hz. At high frequencies, the fact that a two-stage structure is used gives an outstandingly low phase deviation of only −30° at 100kHz.

Fig. 10. Phase Characteristics



Photographs 9 to 14 give the tone-burst response at 10Hz and 10kHz, and the square wave response. The fact that the B-2 is a DC amplifier shows in the almost perfect duplication of the input waveform at 10Hz. The tone-burst and square wave responses at 10kHz are also outstandingly good, and show clearly the influence of the superior high frequency response.

Photograph 14 shows the effect of adding a 0.1μF capacitor in parallel across the 8Ω resistor for the 10kHz square wave response. The superior stability is clearly evident.

Figure 11 shows that the center balance potential drifts only some 10 mV for changes in ambient temperature from 0 to 50°C, indicating the high stability of this DC amplifier.

Fig. 11. Center Potential Drift

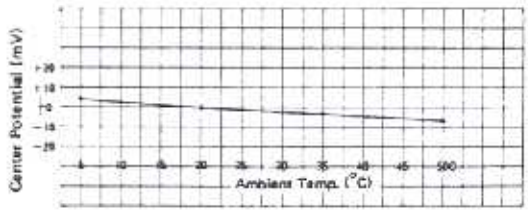


Photo 9

10 Hz Tone Burst and B-2 Response

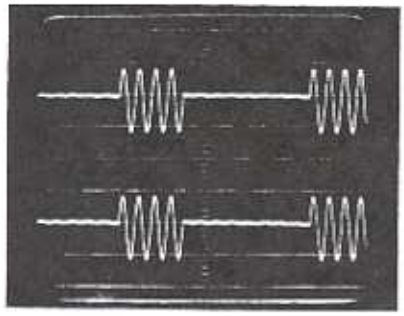


Photo 10

10 kHz Tone Burst and B-2 Response

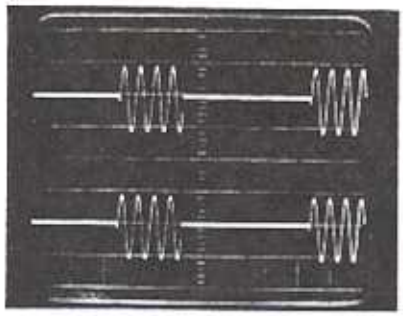


Photo 11

10 Hz Square Wave and B-2 Response

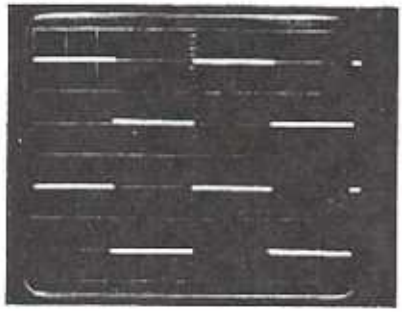


Photo 12

1 kHz Square Wave and B-2 Response

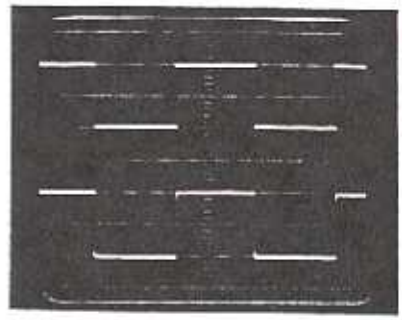


Photo 13

10 kHz Square Wave and B-2 Response

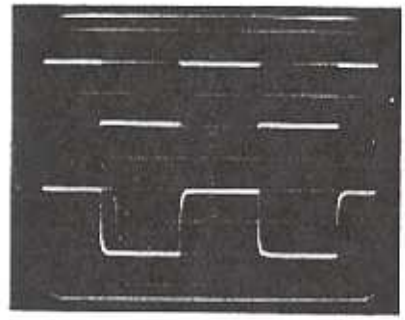
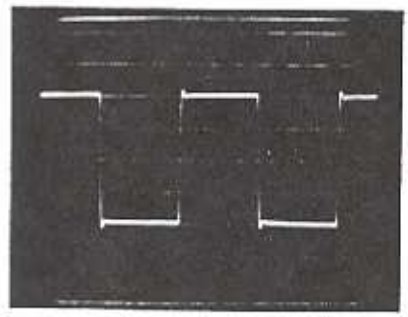


Photo 14

10 kHz Square Wave Response With 0.1 μF Capacitor Across 8Ω Load



3. Electrical Supply Circuit

YAMAHA was the first company in Japan to use separate transformers for the left and right channels (in the B-1) of a power amplifier. The B-2 features the same arrangement, and, to ensure that any unfortunate cross-talk between the two channels is eliminated, each channel uses two 18,000μF electrolytic capacitors (a total of 72,000μF in all). This lifts low frequency response to the highest possible quality.

A full and powerfull bass reproduction is one of the fundamental features of this amplifier. Also, the use of regulated voltage power supplies to the stages before the drive stage, too, with the elimination of any deterioration in S/N ratio due to external noise sources and ripple, is one of the secrets of the extreme stability of amplifier operation. The regulated voltage power supply also includes protective circuits, and is extremely reliable.

4. Automatic Bias Circuit

An automatic bias circuit is used to maintain the power FET bias always at the right value, compensating automatically for the changes in bias voltage which arise from changes in electrical supply voltage. The POWER ON/OFF switch also uses a diode matrix to protect the FETs from high 'rush' currents when switching on.

5. Protective Circuits

• PD Limiter

The B-2 was designed for use with speaker impedances from 4 to 16Ω, but in the unlikely event of a speaker with less than 4Ω being connected, or of an output terminal short circuit, there is full protection for the FETs in the form of a PD limiter which comes into operation when the load impedance drops below 2Ω with more than 50 Watts output. The PD limiter controls the input level in terms of the FET current and voltage detected.

• DC limiter (Speaker Protection)

The B-2 is a DC amplifier, and any DC leakage from preamplifier output terminals would appear as a DC output at the speaker terminals. To eliminate this remote possibility, a special detector circuit is used to detect the DC component in the signal, and to isolate the speaker output terminals by relay to protect the speakers. This relay also operates immediately after switching ON to eliminate the shock noise associated with initial instability.

• Thermally Protected Transformers

Undue rise in transformer temperature is detected and the power supply switched OFF by built-in circuit breakers. Restoration of operation is automatic as soon as the temperature drops to within the permissible range.

• Components Used in the Circuits

The functional elements have been chosen to operate under their optimum conditions, and metallic film resistors, etc., with high temperature stability are used, with gold-plated sliding volume contacts for increased operating reliability.

6. Accessory Circuits

• Peak Level Meters

The meters in the B-2 are essentially those developed for the UC-1 control unit used with the B-1 basic amplifier. They feature an unswitched coverage from −50dB to +5dB (1 mW to 300 W with 8Ω speakers). They use logarithmic compression and give accurate indication of peaks, within 2dB for a single cycle of a 10kHz sine wave.

These high performance meters are available not only to read the B-2 power output levels, but also to read corresponding levels in auxiliary equipment. There is a switch on the rear panel which can be set to EXTERNAL, with option for W/8Ω or 0dBm. On the EXTERNAL W/8Ω setting, the input voltage corresponding to 100 Watts into 8Ω will read 0 VU (100 W) on the meter. This can be invaluable in aligning the output levels for the high frequency, mid frequency, and low frequency amplifiers in a multi-amplifier configuration. On the 0dBm setting, an input of 0.775 V rms will read 0dB, which is convenient for reading preamplifier outputs, etc.

Fig. 12. Peak Level Meter Response

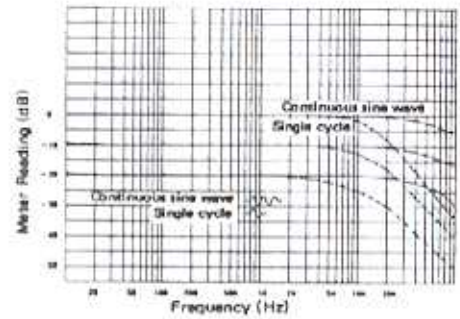
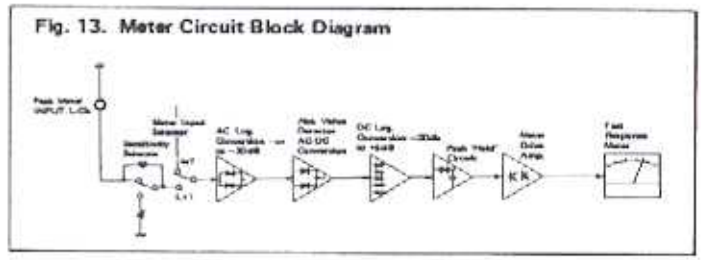


Fig. 13. Meter Circuit Block Diagram



• Selection of Two Speaker Systems with Level Control

Selection of either of two sets of speakers may be made by selector switch on the front panel, and the level for each of the four speakers set independently by volume type controls. It is possible to test-compare speakers with different efficiencies at the same listening level. The method used inserts an attenuator before the power amplifier input, and results in virtually no degradation of the output quality. Also, the speaker ON/OFF switch leaves the meter operative, so that output power can be measured, even when the speakers are OFF, and so that levels can be checked before connecting the output to the speakers. Again, two separate inputs can be selected by switch on the front panel.

• Input Switch

The availability of two input circuits is very convenient: one can be used for full-range reproduction, and the other, via a frequency divider network, for multi-amplifier applications. Or one of the two inputs can be shorted, so that the selector operates as an input ON/OFF switch.

B-2 SPECIFICATIONS

Power Amplifier Section

Feature	Conditions	Specification
Dynamic Power	8Ω, 1kHz, 0.1% THD	140 + 140 Watts
Rated Power	8Ω, 20Hz to 20kHz 0.08% THD	100 + 100 Watts
	4Ω, 20Hz to 20kHz 0.08% THD	140 + 140 Watts
Phase Deviation	DC to 100kHz, (at 10 Watts)	+0 to −30°
Power Bandwidth	3 dB down, at 0.5% THD, 8Ω	5Hz to 100kHz (IHF)
Damping Factor	20Hz 8Ω	70
	1kHz 8Ω	70
	20kHz 8Ω	50
Total Harmonic Distortion	20Hz to 20kHz, rated output 8Ω	Less than 0.08%
	20Hz to 20kHz, 50 Watts output 8Ω	Less than 0.01%
	20Hz to 20kHz, 10 Watts output 8Ω	Less than 0.008%
Intermodulation Dist.	70Hz : 7kHz = 4 : 1 at 50W, 8Ω	Less than 0.03%
	70Hz : 7kHz = 4 : 1 at 50W, 4Ω	Less than 0.03%
	70Hz : 7kHz = 4 : 1 at 50W, 16Ω	Less than 0.03%
Frequency Response	1 Watt output, 8Ω, DC setting	DC to 100kHz $^{+0}_{-1}$ dB
	1 Watt output, 8Ω, NORMAL setting	10Hz to 100kHz $^{+0}_{-1}$ dB
Input Impedance		25kΩ
Input Sensitivity		775mV
Signal-to-Noise	IHF-A, 4.7kΩ input short	115 dB
Residual Noise		0.25mV
Input Terminals		1, 2 (Front panel switch)
		NORMAL/DC (Rear panel switch)
Output Terminals		A, B (Rear panel switch)

Peak Meter Section

Feature	Specification
Meter Range	–50 to +5 dB (0 dB = 8Ω/100W or 0 dB = 0 dBm)
Accuracy	+5 to –20 dB ±1.0 dB –20 to –40 dB ±2.0 dB –40 to –50 dB ±3.0 dB
Frequency Response	20Hz to 20kHz ±1.0 dB
Rise/Decay Time	100 μsec/1 sec
Input Terminals	RCA pin jacks for EXTERNAL
Indicator Switch	INTERNAL/EXTERNAL on rear panel
Sensitivity/Input Impedance	0 dB = 8Ω/100 Watts (INTERNAL) 0 dB = 8Ω/100 Watts/100kΩ 0 dB = 0 dBm/43kΩ } (EXTERNAL)

General

Semiconductors	8 Vertical FETs, 4 Horizontal FETs 95 Bi-polar Transistors, 2 ICs, and 66 Diodes (including LEDs).
Power Consumption	290W
Dimensions (W x H x D)	436mm (17-1/8") x 370mm (14-5/8") x 151mm (6")
Weight	26kg (57lb 3oz)